In the Claims:

1. (currently amended) A test architecture within an integrated circuit comprising;

A. a plurality of core wrappers each having a serial input, a serial output, and control inputs, the control inputs including a clock input, a shift input, a capture input, an update input, a reset input, an enable input, and a core select input;

B. input circuitry having a serial input, a plurality of serial outputs, each selectively coupled to the serial input, and control inputs, each serial output being connected to the serial input of a core wrapper;

C. output circuitry having a plurality of serial inputs, a serial output, and control inputs, each serial input being connected to the serial output of a core wrapper and each serial input being selectively coupled to the serial output; and

D. a link instruction register having a serial input, a serial output, control inputs, and control outputs,

i. the control inputs including a clock input coupled to the clock input of the core wrappers, a shift input coupled to the shift input of the core wrappers, a capture input coupled to the capture input of the core wrappers, an update input coupled to the update input of the core wrappers, and a link select input coupled to the select input of the core wrappers,

ii. the control outputs including plural enable outputs, each enable output being coupled to the enable input of a core wrapper,

iii. the serial input and the serial output of the link instruction register being connected in series with the serial input of the input circuitry and the serial output of the output circuitry, and

iv. the link instruction register including an instruction register connected to the serial input and to

the control outputs, and a multiplexer connected to the serial input, the serial output, and the select input.

2-9. (canceled)

10. (previously presented) The test architecture of claim 1 in which the integrated circuit is formed on a semiconductor substrate.

11. (previously presented) The test architecture of claim 1 in which the instruction register includes a shift register selectively connected in series between the serial input and the serial output of the link instruction register.

12. (previously presented) The test architecture of claim 1 in which the instruction register includes a shift register, an update register, and decode logic.

13. (previously presented) The test architecture of claim 1 in which the link instruction register includes a logic gate selectively controlling at least some of the control inputs in response to a select signal on the select input.

14. (previously presented) The test architecture of claim 1 in which the link instruction register includes a logic gate selectively controlling the control inputs, except for a reset signal on a reset input, in response to a select signal on the select input.

15. (previously presented) The test architecture of claim 1 in which the instruction register has a serial input connected to the serial input of the link instruction register and a serial output selectively connected to the serial output of the link instruction register by the multiplexer.